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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Mostafazadeh, Shahram; Smith, Joseph O.		
Assignee:	National Semiconductor Corp.		
Title:	Lead Frame Chip Scale Package		
Serial No.:	Unassigned	Filing Date:	Herewith
Examiner:	Unknown	Group Art Unit:	Unknown
Docket No.:	NS-3877-2D US		

San Jose, California
July 25, 2000

BOX PATENT APPLICATION
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above-referenced patent application as follows:

IN THE CLAIMS

Please cancel Claims 1-10.

Please add Claims 11-17 as follows:

11. An integrated circuit package for accommodating a semiconductor die, comprising:

a lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads having a lower surface that is substantially coplanar with said lower surface of said die attach

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